SECTION 6.
TECHNICAL DESCRIPTION

6.1 RECEIVER

The RF signal enters the receiver at CN5P, passes through bandpass filter BPF1, RF amplifier Q101, and BPF2, to mixer DBM1. Here it is mixed with the local oscillator signal to become the first IF of 21.6 MHz. This signal is amplified and filtered by Q102, Q103, XF101 and XF102, and finally, IC107 which provides conversion to a low IF of 455 kHz, limiting, audio detection and squelch processing.

The audio signal is separated into the standard audio signal and the high frequency noise component which is detected and used for squelch operation.

6.1.1 AUDIO

The Audio output of IC107 passes to buffer IC108A. Jumper JP102 allows audio to be passed through an optional CTCSS decoder. Q106, Q107, Q108, IC109 and associated components provide a 100 ms, delay to the audio. This eliminates annoying "squelch tail" by allowing sufficient time for the squelch circuit to turn off the audio path before the noise burst occurs. This system is effective for both noise-squelch and CTCSS radios. Q106 and Q107 comprise a multivibrator providing a clock signal of 12 kHz to IC109 which is a bucket brigade delay device. Q108 and associated components remove the clock signal and pass the delayed audio to IC110B, the de-emphasis network, and IC110A. FVR101 provides adjustment for de-emphasis at 3 kHz. The audio then passes through squelch gate Q111 to amplifier IC111. FVR102 adjusts the level of the audio. CN102 pin 8 provides a low level audio signal of approximately -6 DBM (to ground) while CN102 pin 9 provides speaker level audio from IC116 audio PA.

6.1.2 SQUELCH

High frequency noise is amplified by IC108B and detected by D110. Diode bias is adjusted by FVR103 squelch control. In some applications, this control may be remoted to an external control unit. The recovered DC squelch voltage is amplified by IC107, Q104 and inverted by switch Q105. When the squelch is open (on signal), Q105C goes high.

Q111 is the squelch gate which breaks the audio path upon command from the squelch and/or CTCSS circuits. The squelch signal (high) enters through D113 to turn on the gate. The AF LOCK signal originates in the CTCSS and is low until the proper tone is received. This low holds the gate closed. The squelch signal is also made available to the control connector as a BUSY signal.

6.1.3 SIMPLEX/DUPLEX

The radio is capable of either simplex or full duplex operation. If jumper JP101 is in place, the PRESS (push-to-talk) line is connected to Q109/Q110 which acts as a power switch to turn off the receiver during transmission. If JP101 is removed, full duplex operation is allowed.

6.2 PLL SECTION

The PLL sections of the transmitter and receiver are identical with the exception that the receiver PLL contains the 12 MHz TCXO and IC106 divider (16) to produce the 750 kHz reference signal. This signal is shared by both TX and RX. IC105/305 provides further division to obtain latch signals for the PLL chip IC103/303 and address data for the EPROM (A_0, A_1, A_2). Additional address data is provided by the channel select bus A_3 thru A_9 allowing a selection of up to 128 channels. Note that separate EPROMs are used for TX and RX allowing totally independent programming.

The EPROM supplies R, N and A data to the PLL via buffer IC102/302 which controls the divisions within the PLL. R specifies the division rate of 750 kHz strobe signal to provide the final reference signal to the phase detector. N specifies the main division rate of the 10 bit counter, while A specifies the fractional division for the 7 bit counter. The result of the final division is applied to the phase detector along with the reference signal.

Phase detector output is passed through a low pass filter to the VCO at CN103S/305S.

Pin 13 provides the unlock (LOW)signal. On RX, this lights LED D106 via Q112 and shuts down the VCO LO output to the receiver. On TX, it shuts down the drive as well as the VCO output.

6.3 RECEIVER VCO

The PLL control voltage applied to CN103P pin 2 controls the frequency of oscillator Q201 by changing the capacitance of varactor D201. L202(VHF), VC201(UHF) adjusts VCO centering. The VCO operates at carrier frequency. Oscillator output is amplified by IC201 and supplied: (1) back to the PLL prescaler and (2) to Q202 for additional amplification and application to the receiver as a local oscillator signal.

If the PLL drops out of lock, the voltage at CN103P pin 5 drops turning Q204 on and Q203 off. This switches off power to amplifier Q202 and removes the local oscillator signal, preventing any spurious responses during unlock.

In the simplex mode, the PRESS (push-to-talk) applied to CN103P pin 7 as a "low" turns on Q206 biasing Q205 to cut-off. This removes power from the oscillator and removes bias from amplifier Q202 disabling the local oscillator and the receiver front end. In the duplex mode, jumper JP101 disconnects the PRESS line from the VCO allowing the receiver to operate during transmit.

Q207 provides filtering while Q208/D206 act as a voltage regulator supplying 5 volts to amplifier IC201.

6.4 TRANSMIT VCO

In the transmit mode, the press signal applied to CN305P pin 7 as a "low" turns on Q405. This applies power to the oscillator and supplies bias to amplifier Q402.

The PLL control voltage applied to CN305P pin 2 controls the frequency of oscillator Q401 by changing the capacitance of varactor D401. VC401(UHF) adjusts VCO centering. The VCO operates at carrier frequency. Oscillator output is amplified by IC401 and supplied: (1) back to the PLL prescaler and (2) to Q402 for additional amplification and application to the transmitter as a drive signal.

If the PLL drops out of lock, the voltage at CN305P pin 5 drops, turning Q404 on and Q403 off, removing power from amplifier Q402. This removes the drive signal, preventing any spurious transmission during unlock.

Q406 provides filtering while Q407/D404 act as a voltage regulator supplying 5 volts to amplifier IC401.

The audio signal from the modulator section is applied through CN305P pin 1 to varactor D401B, thereby providing frequency modulation of the VCO.

6.5 TRANSMITTER

The VCO output at CN306 is amplified by driver stages Q301 and Q302 and fed to the PA at CN7P. These are wide band amplifiers requiring no tuning. A portion of the RF present at the output is detected by D314 and D315 and is available at CN303S pin 6 as an analog indication of drive level.

Q303, IC308 and FVR301 control the output of the driver by adjusting the collector voltages of Q301 and Q302. This voltage may be monitored at TP303. In the receive mode, or if an unprogrammed channel is selected (VCO out of lock), Q304 is turned off by the unlock line (low). This turns off Q303 and turns off power to the driver stages.

Q305 and Q306 are switches which transfer the PRESS command to the VCO and PA sections to enable these circuits.

6.6 MODULATION SECTION

Transmit audio at -34dBm is applied at CN303S 1 (HI) and 2 (GND). FVR304 sets the level applied to AGC amp IC310. Buffer amplifier IC309A drives the preemphasis shaping network. A 6dB/octave slope is created from 300 Hz to over 3 kHz. Audio from the 5 tone selective call system is introduced at this point. IC309B provides adjustable gain and supplies audio signal to FVR302 modulation level control. The CTCSS encode signal is introduced at this point. L310, 311 and associated capacitors provide a steep roll-off of frequencies above 3 kHz. The processed composite audio signal is supplied to the VCO via CN305, pin 1.

6.7 TRANSMITTER PA

PA input is amplified by IC601 and Q601 and supplied to the output port through the low-pass filter. Control circuits regulate power under conditions of varying input voltage and reduce drive with excessive heat-sink temperature.

The power control circuit consists of Q602 series regulator, Q603 [PTT] switch, Q604 regulator driver, Q605 temperature sense amplifier, IC601A control amplifier and associated components.

Power level is detected by D602 and supplied to control amplifier IC602A, Q604 and on to regulator Q602. Any change in power will result in a correction at the driver restoring power output to the proper level.

Power adjustment FVR601 sets the power output level of the transmitter. This control provides input to IC602A for power control.

PA temperature is sensed by posistor PS601 which controls the base bias of Q605. This provides another input to IC602. Excessive heat-sink temperature will result in reduced power.

When the PRESS (push-to-talk) line is high, Q603 is turned off causing the power control circuit to disable the transmitter.

IC602B serves as the TX LED driver. When RF is sensed by D602, pin 1 goes positive, turning on the TX LED. Note that the LED will not light unless the unit is actually putting out power.

6.8 CONTROL UNIT

The unit contains the following circuits which will be described individually:

A. Microphone AGC and buffer amplifiers

B. Speaker

C. Power switch

D. Volume control

E. Squelch control

F. Channel selector and indicator

G. Tone select switches and indicators

H. Voltage regulator

I. TX LED

J. BUSY LED

6.8.1 MICROPHONE CIRCUIT

The microphone connects to the control unit through a seven pin connector. Table 6-1 shows the pinout.

Table 6-1. Microphone Circuit

PIN	FUNCTION
1	Microphone audio high
2	Microphone audio ground
3	Reset (used with decoders)
4	Press [PTT] switch
5	Monitor (CTCSS disable)
6	Call (used with 5 Tone Select Call)
7	Ground

R404 and C402 provide filtered B+ for mike bias. R403, input level control FVR401, and R401 are the collector load for the preamplifier contained in the mike. R402 works with these components to act as a voltage divider. Audio from FVR401 passes through C403 into AGC amp IC401 pin 3 and out pin 5. Power, 8VDC, is applied at pin 1. Output is coupled through C406 to AGC detector input, pin 6, as well as through C407 to output level control FVR402. RC networks at pins 2 and 4 are time constants for the AGC. IC402 a and b provide a balanced 600 ohm output through R413/C410 to CN6P-20 and R414/C411 to CN6P-21. Use of a balanced line minimizes noise pickup on the cable when the optional trunk mount kit is used.

The CALL line may be used to provide 8 VDC to the mike jack for use by DTMF microphones and other input devices requiring operating voltage. This is done using jumper JP806 on the options board. If this is done, caution must be used. In the event a microphone is connected which has a CALL button, pressing this button will cause a short circuit condition. If this causes concern or is likely to happen, use a 120 Ohm 1 Watt wire wound resistor instead of JP806 to limit the short circuit current to a safe value.

6.8.2 SPEAKER

The speaker is driven through a resistive network, R415, R416, R417, which reduces the applied power to the limit of the small, internal speaker.

6.8.3 POWER SWITCH

The power switch provides a ground to a relay in the main chassis. This controls power to all circuits except the RF power amplifier which is connected directly to the battery supply.

6.8.4 VOLUME CONTROL

The volume control sets the gain of amplifiers contained in the main chassis.

6.8.5 SQUELCH CONTROL

The squelch control adjusts the gain of a noise amplifier contained in the main chassis.

6.8.6 CHANNEL SELECTOR AND INDICATOR

Channel selector switch S401 provides the four bit code for the PLL as well as the seven segment codes for the channel indicator displays. An 8V high connects to the switch common which selectively pulls up the outputs as dictated by the position of the switch. The ground for the displays returns to CN6P-29, LED COM. In the KG105 this is driven by a dimmer/flashing circuit in the main chassis. In the KG106, it is grounded.

6.8.7 TONE SELECTORS AND INDICATORS

The tone switches are used to select encode and decode tones for the CTCSS option. If the five-tone selective call option is installed, the switches select the last two digits of the called number. The circuit provides two, four bit binary codes to the main chassis for processing by these options.

S403 and S404 are momentary switches which provide a momentary low to Schmitt triggers, IC404 for debounce and inversion and on to IC405 which is a dual BCD up-counter. Pulses from S403 increment the counter for the X1 (second) digit of the indicator while S404 increments the X10 (first) digit. The BCD outputs of the counter are applied to IC407 and IC408 which are BCD to seven-segment decoder/drivers for the indicators. The BCD counter outputs are also applied to IC406 which is a data selector. A logic low input on the AK line, pin 7, selects the X1 data while a low on the BK line will select the X10 data. This provides separate codes for encode and decode when CTCSS is used. The indicators remain lighted regardless of the data selected. D401 and C417 provide a short term voltage supply for the circuit so that the codes are held for brief power interruptions (less that one minute).

CN6P pin 8 serves to blank the tone displays when they are not required as when neither the selectable CTCSS nor the five-tone options are installed. This is done using the blanking inputs to the driver ICs. A logic low will light the displays. If left open, the line floats high and the displays light.

6.8.8 VOLTAGE REGULATOR

IC403 provides a source of regulated 8 Volts to all active circuits in the control unit.

6.8.9 TX LED

The TX LED is driven by a voltage from the main chassis when the unit is in the transmit mode. In the KG105 this voltage originates in the transmitter PA and appears only when power is present. In the KG106 the voltage is supplied by control logic in the main chassis.

6.8.10 BUSY LED

The BUSY LED is driven by the squelch circuit in the main chassis. The busy line goes high on the reception of a signal.

6.9 HANDSET

The electrical and electronic circuitry of the DTMF handset is contained on four separate circuit boards. Most of the circuitry is contained on the main circuit board in the handset, with most of the remainder located on the base unit circuit board.

6.10 BASE UNIT

The circuitry in the base unit provides the speaker switching functions as well as [PTT] and Channel Monitor switching functions.

Referring to the base unit schematic on page 85, the circuit comprised of U301, U303, and U304 as well as R301-R315 functions as a four-state control line decoder. This control line circuitry decodes the four possible DC voltage at J301-4 which originate on the handset PC board (see section 6.11). The results of this decoding process are used to actuate the [PTT] output transistor Q303 and the Channel Monitor output transistor Q302, as well as the speaker relay control transistor Q301.

Voltage regulator U302 supplies +5V power to all circuitry on this board except the relay and the quad comparator U301. JMP1 is used in conjunction with some harness installations and with decoder PC boards which are mounted in the base unit. This jumper position is shorted with a jumper wire in most installations, as are wire pads E301 and E305.

L301, L302, C301, C303-C305, C307, R323, and R324 are all used in input or output filter networks for Radio Frequency Interface (RFI) suppression. Diodes CR301, CR303 and CR304 are used as input voltage limiters and static protection devices. Diode CR302 is used to suppress voltage spikes from relay K301. Wire attachment pads E301-E315 allow the installation of a DTMF decoder module (not supplied) inside the base unit.

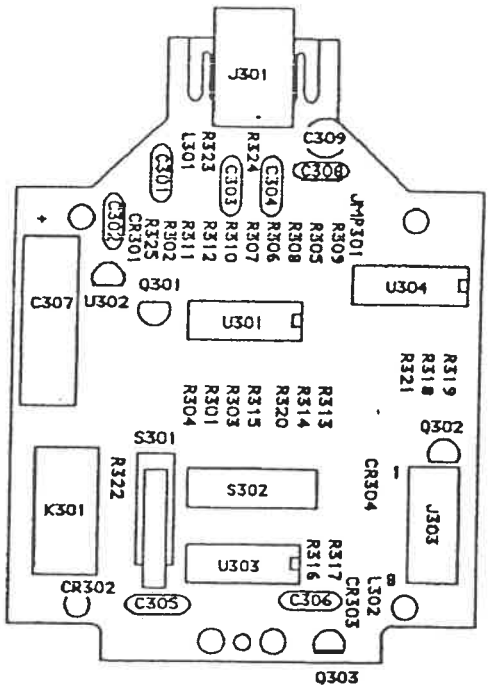

Figure 6-3. Handset Base Unit Component Layout

6.11 HANDSET CIRCUIT DESCRIPTIONS

The circuitry in the handset is used to provide interfacing among the microphone, earpiece speaker, [PTT] switch, radio speaker control switch, and the radio itself via the base unit previously described. Microcontroller U1 (along with EPROM U2 and resistor network RN1) performs all control functions in the handset. Inputs to U12 are taken from the [PTT] switch, keypad and hook switch. Outputs from U1 include DTMF and "beep" tones (via the D/A convertor action of RN1), [PTT] requests, and Channel Monitor line control, with the last two functions carried into the base unit logic section via the four-state control line circuitry described below.

Transistor Q1 and Q2 along with diode CR3, capacitor C2, and resistors R3-R6 form a low-voltage reset circuit, inhibiting operation of U1 at supply voltages below about 7.5 VDC. U1 has an internal 3.58 MHz clock oscillator which uses Y1, C3, C4, and R7 as a feedback network.

Quad operational amplifier sections U4A and U4B are used to amplify and condition microphone audio as well as to amplify DTMF audio from the microcontroller D/A convertor network (RN1). U4C is used to provide isolation between the transmitter audio circuitry and the earpiece amplifier U5. U4D is used as a voltage follower, with the purpose of driving the 4-state control line with voltages obtained from the junction of the 2-bit

D/A convertor resistors R37 and R38. The voltages on this control line are listed here for reference:

Table 6-2 Control Line States

J1-4 VOLTAGE (VDC)	HANDSET OPERATIONAL STATE
0.0	Speaker switch "off", [PTT] button released, no keypad buttons pressed.
1.7	Speaker switch "on", [PTT] button released, no keypad buttons pressed.
3.3	Speaker switch "on" or "off", [PTT] button pressed In, keypad buttons either pressed or not pressed.
5.0	Speaker switch "on" or "off", [PTT] button released, any keypad button pressed.

NOTE:

The above voltages are present when Handset DIP switch S4 sections 6 and 7 are "on" and sections 8 and 9 are "off". The positions of the other handset and base DIP switches should not affect the above values.

Cermet potentiometer RV1 controls the DTMF audio level to the transmit audio mixing circuitry, while RV2 and RV3 control the microphone sidetone level and microphone output level, respectively. RV4 and S4-4 allow adjustment of the receiver input level, with CR4 and CR5 limiting this audio signal to a safe value for U5.

U6, U8, and U9 form a logic network which takes as input the positions of switches S101 ([PTT] switch), S2, S3, S4-5 through S4-8, and U1-19 (microcontroller transmit request output). The outputs from this network are used to control microphone and sidetone muting, the [PTT] LED, and four-state control line D/A convertor. This network also functions as an automatic [PTT] latching circuit when enabled by DIP switch sections S4-7 and S4-8.

Voltage regulator U3 supplies +5VDC to all of the integrated circuits on this board except U4, which is powered from the unregulated 8-16 V line. L1, C10, C11, C26, R40, and R41 serve as RFI suppression components. Jack J5 allows the connection of an optional LCD display module (not yet available).

The following table shows the row and column tone frequencies generated by the handset in normal DTMF dialing operations:

Table 6-3. DTMF Tone Frequencies

TONE GROUP	TONE FREQUENCY (Hz)		PERCENT DEVIATION *
	(TELCO STANDARD)	HANDSET	
Row 1	697.0	699.1	+0.30
Row 2	770.0	766.2	-0.49
Row 3	852.0	847.4	-0.54
Row 4	941.0	948.0	+0.74
Column 1	1209.0	1215.9	+0.57
Column 2	1336.0	1331.7	-0.32
Column 3	1477.0	1471.9	-0.35
Column 4	1633.0	1645.0	+0.73

* Percent Deviation does not include crystal oscillator frequency errors. The EIA-470A standard for frequency deviation is plus or minus 1.5%.